

CLAIMS

What is claimed is:

- 1 1. A data-retention circuitry comprising:
2 data-retention subcircuits in a feedback loop; and
3 a supply-switching subcircuit to provide current to the data-retention
4 subcircuits from a supplemental voltage supply through a well tap during a
5 standby mode.
- 1 2. The data-retention circuitry of claim 1 further comprising an isolation
2 subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in
3 response to a sleep signal,
4 wherein the supply-switching subcircuit is to switch from a regular
5 voltage supply to the supplemental voltage supply in response to the sleep signal,
6 and
7 wherein the isolation subcircuit is to pass data signals between the data-
8 retention subcircuits and the pass-gate subcircuit when voltage from the regular
9 voltage supply is present.
- 1 3. The data-retention circuitry of claim 1 wherein the data-retention
2 subcircuits are to retain a state when receiving current from the supplemental
3 voltage supply.
- 1 4. The data-retention circuitry of claim 2 wherein the pass-gate subcircuit
2 is to pass a latched state signal to the isolation subcircuit in response to a clock
3 signal.
- 1 5. The data-retention circuitry of claim 2 wherein the data-retention
2 subcircuits, the switching subcircuit and the isolation subcircuit comprise lower-
3 leakage semiconductor devices.

1 6. The data-retention circuitry of claim 2 wherein the data-retention
2 subcircuits are coupled in series in the feedback loop, and wherein the data-
3 retention circuitry comprises an output inverter to receive a state signal from one
4 of either the isolation subcircuit or the pass-gate subcircuit and to provide an
5 output signal.

1 7. The data-retention circuitry of claim 1 wherein the supply-switching
2 subcircuit comprises a semiconductor switching subcircuit that is part of a
3 semiconductor die, the semiconductor die having a well-tap to provide the current
4 from the supplemental voltage supply, and
5 wherein the semiconductor switching subcircuit is to couple the data-
6 retention subcircuits to the regular voltage supply when the semiconductor
7 switching subcircuit receives a first state of the sleep signal, and wherein current
8 is to flow to the data-retention subcircuits from the well-tap when the
9 semiconductor switching subcircuit receives a second state of the sleep signal.

1 8. The data-retention circuitry of claim 2 wherein the regular and
2 supplemental voltage supplies are provided by a single voltage source, the regular
3 voltage supply being decoupled from the supplemental voltage supply during the
4 standby mode.

1 9. The data-retention circuitry of claim 2 further comprising a master latch
2 to latch a state signal, and wherein the pass-gate subcircuit, the data-retention
3 subcircuits, the isolation subcircuit and the supply-switching subcircuit are part of
4 a slave latch, and
5 wherein the pass-gate subcircuit is to pass the latched state signal to the
6 isolation subcircuit from the master latch in response to a clock signal.

1 10. The data-retention circuitry of claim 9 wherein circuits of the master
2 latch are to receive power from the regular voltage supply, and wherein during the
3 standby mode the regular voltage supply is turned off.

1 11. The data-retention circuitry of claim 9 wherein the data-retention
2 subcircuits, switching subcircuit and the isolation subcircuit comprise lower-
3 leakage semiconductor devices, and wherein the pass-gate subcircuit and master
4 latch comprise higher-leakage semiconductor devices, the lower-leakage devices
5 having at least one of either a longer channel length, a thicker gate-oxide layer or a
6 higher threshold voltage than the higher-leakage semiconductor devices.

1 12. A processing system comprising:
2 a processor on a semiconductor die; and
3 a data-retention circuitry on the semiconductor die to retain state
4 information for the processor during a standby mode, wherein the data-retention
5 circuitry comprise data-retention subcircuits to receive current through a well tap
6 in the semiconductor die during the standby mode to retain the state information.

1 13. The system of claim 12 wherein the data-retention circuitry further
2 comprise an isolation subcircuit to isolate the data-retention subcircuits from a
3 pass-gate subcircuit in response to a sleep signal, and a supply-switching
4 subcircuit to provide current to the data-retention subcircuits from a supplemental
5 voltage supply through the well tap during the standby mode.

1 14. The system of claim 12 wherein the data-retention circuitry are
2 arranged in cells on the semiconductor die, the cells having at least one well tap to
3 provide the current from the supplemental voltage supply of an associated one of
4 the cells.

1 15. The system of claim 13 wherein the supply-switching subcircuit is to
2 switch from a regular voltage supply to the supplemental voltage supply in
3 response to a sleep signal, and
4 wherein the isolation subcircuit is to pass data signals between the data-
5 retention subcircuits and the pass-gate subcircuit when voltage from the regular
6 voltage supply is provided.

1 16. The system of claim 13 wherein the pass-gate subcircuit is to pass a
2 latched state signal to the isolation subcircuit in response to a clock signal.

1 17. The system of claim 16 wherein the data-retention circuitry further
2 comprise a master latch to latch a state signal, and
3 wherein the pass-gate subcircuit, the data-retention subcircuits, the
4 isolation subcircuit and the supply-switching subcircuit are part of a slave latch,
5 and
6 wherein the pass-gate subcircuit is to pass the latched state signal to the
7 isolation subcircuit from the master latch in response to a clock signal.

1 18. The system of claim 17 wherein circuits of the master latch are to
2 receive current from the regular voltage supply, and wherein during the standby
3 mode the regular voltage supply is turned off.

1 19. The system of claim 17 wherein the data-retention subcircuits,
2 switching subcircuit and the isolation subcircuit comprise lower-leakage
3 semiconductor devices, and wherein the pass-gate subcircuit and the master latch
4 comprise higher-leakage semiconductor devices, the lower-leakage devices having
5 at least one of either a longer channel length, a thicker gate-oxide layer or a higher
6 threshold voltage than the higher-leakage semiconductor devices.

1 20. A method comprising:
2 isolating data-retention subcircuits in response to a sleep signal;
3 switching the data-retention subcircuits to receive current from a
4 supplemental voltage supply in response to the sleep signal; and
5 retaining state information by the data-retention subcircuits when receiving
6 the current from the supplemental voltage supply during a standby mode.

1 21. The method of claim 20 further comprising providing the current from
2 the supplemental voltage supply through a well-tap on a semiconductor die.

1 22. The method of claim 20 wherein switching further comprises
2 switching from a regular voltage supply to the supplemental voltage supply in
3 response to the sleep signal.

1 23. The method of claim 22 further comprising passing state information
2 between the data-retention subcircuits and a pass-gate subcircuit when the regular
3 voltage supply is present at an isolation subcircuit.

1 24. A wireless communication device comprising:
2 an omnidirectional antenna to communicate radio-frequency signals;
3 a processor on a semiconductor die to convert between the radio-frequency
4 signals and data signals; and
5 a data-retention circuitry on the semiconductor die to retain state
6 information for the processor during a standby mode, wherein the data-retention
7 circuitry comprise data-retention subcircuits to receive current through a well tap
8 in the semiconductor die during the standby mode to retain the state information.

1 25. The device of claim 24 wherein the data-retention circuitry further
2 comprise an isolation subcircuit to isolate the data-retention subcircuits from a
3 pass-gate subcircuit in response to a sleep signal, and a supply-switching
4 subcircuit to provide current to the data-retention subcircuits from a supplemental
5 voltage supply through a well tap during the standby mode.

1 26. The device of claim 25 wherein the data-retention subcircuits,
2 switching subcircuit and the isolation subcircuit comprise lower-leakage
3 semiconductor devices, and wherein the pass-gate subcircuit comprises higher-
4 leakage semiconductor devices, the lower-leakage devices having at least one of
5 either a longer channel length, a thicker gate-oxide layer or a higher threshold
6 voltage than the higher-leakage semiconductor devices.